ABSTRACT

The present invention relates to a particular single cell erasing method for recovering memory cells under reading or programming disturbs in non volatile semiconductor memory electronic devices comprising cell matrix split in sectors and organized in rows, or word lines, and columns, or bit lines.

This kind of memory devices generally provides the application of a sector erasing algorithm with subsequent testing phase (erase-verify); but the method according to the present invention provides a bit by bit erasing by applying to each single word line a negative voltage used during the erasing of a whole sector and on the drain terminal of each single cell a programming voltage.

With this kind of selective bias it is possible to perform a single cell, or bit by bit, erasing, allowing all the cells in case under a reading or programming disturb increasing the original threshold value thereof to be recovered.